REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 1-20 are pending in the application. Independent claim 1 has been amended to better define the claimed invention. Support for amended claim 1 is found in the application as filed, especially FIGs. 4-5. New claims 11-20 have been added to provide Applicants with the scope of protection to which they are believed entitled. Support for the added claims is found in the application as filed, especially the original claims and FIGs. 3-4. The Abstract has been revised to be compliant with commonly accepted US patent practice. No new matter has been introduced through the foregoing amendments.

The Examiner rejected claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over *Tatsuta et al.* (U.S. 6,713,844) in view of *Kurogi et al.* (U.S. 5,578,874). The rejection is erroneous because the applied references, especially *Tatsuta*, clearly fail to teach or suggest all limitations of the rejected claims, especially, the claimed **multi-layer** ceramic structure of original claim 1. It is acknowledged that *Tatsuta* teaches a ceramic substrate 1. However, ceramic substrate 1 of *Tatsuta* is obtained by performing injection molding with use of a mixture of a ceramic powder and a binder, and sintering a resultant molded article. *See* column 3, lines 52-55 of *Tatsuta*. Thus, substrate 1 of *Tatsuta* cannot have the claimed multi-layer structure. The obviousness rejection of claims 1-10 is therefore inappropriate and should be withdrawn.

Notwithstanding the above, Applicants have amended independent claim 1, solely for the purpose of expediting prosecution, to further distinguish the claimed invention from *Tatsuta*.

Amended claim 1 is directed to a package structure with a cavity, which comprises a chip having a circuit disposed thereon and a plurality of first bonding pads disposed around the circuit,

and the first bonding pads being electrically connected to the circuit; a multi-layer ceramic substrate having a hollow formed therein and a plurality of second bonding pads disposed around the hollow and electrically connected to the first bonding pads, wherein the hollow and the plurality of second bonding pads correspond to the circuit and the plurality of first bonding pads, respectively; and an adhesive layer formed around the hollow and between the chip and the multi-layer ceramic substrate for tightly bonding the chip and the multi-layer ceramic substrate together, *wherein the chip, the adhesive layer and the hollow of the multi-layer ceramic substrate together define a cavity such that the circuit of the chip is disposed within the cavity*.

Tatsuta et al. (U.S. 6,713,844) teach a 1st embodiment in which a semiconductor chip (2) is mounted on a substrate (1), and a resin material (3) is filled and cured in a space between the substrate and the semiconductor chip (See column 3, lines 55-61 and FIGs. 1A-3B). However, the resin material 3c illustrated in FIGs. 1A-3B is filled and cured in the whole space between the substrate and the semiconductor chip *without any cavity left*. In a 2nd embodiment, *Tatsuta et al.* teach a concave 17 (See FIGs. 7A-10B) is formed on the substrate 1, and the chip 2 is disposed on the projections 11 within the concave 17. However, *Tatsuta et al.* still fail to teach or suggest the features *"an adhesive layer formed around the hollow and between the chip and the multi-layer ceramic substrate for tightly bonding the chip and the multi-layer ceramic substrate together"*, and *"the chip, the adhesive layer and the hollow of the multi-layer ceramic substrate together define a cavity such that the circuit of the chip is disposed within the cavity"* as recited in amended claim 1. Further, *Kurogi et al.* (U.S. 5,578,874) merely teach a substrate having a number of via conductors formed therein. Accordingly, Applicant respectfully submits that the cited references, singly or in combination, fail to teach or suggest the newly claimed features of amended claim 1.

Therefore, amended claim 1 is nonobvious over the cited references. If an independent claim is nonobvious under 35 USC 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Claims 2-11 and 18-20 depend from

independent claim 1, and thus the citations fail to render them unpatentable.

Claims 2-11 and 18-20 are also believed patentable on their own merits since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art.

For example, as to claim 2, Applicants respectfully disagree with the Examiner's allegation that the term "SAW" (Surface Acoustic Wave) simply sets forth the intended use of the claimed chip. A person of ordinary skill in the art would recognize that the term SAW chip structurally defines a chip that has a piezoelectric component which produces or excites surface acoustic waves. The applied references disclose no such component or SAW chip and therefore do not render obvious claim 2.

As to claim 5, Applicants respectfully disagree with the Examiner's allegation that the term "crystal" simply sets forth the intended use of the claimed chip. A person of ordinary skill in the art would recognize that the term "crystal" is a structural limitation, rather than a functional citation. The applied references disclose no such crystal structure and therefore do not render obvious claim 5.

As to claim 6, Applicants respectfully disagree with the Examiner's allegation that the term "MEMS" (MicroElectroMechanical Systems) simply sets forth the intended use of the claimed chip. A person of ordinary skill in the art would recognize that the term MEMS chip structurally defines a chip that has one or more moving component. The applied references disclose no such component or MEMS chip and therefore do not render obvious claim 6.

As to claim 18, the applied references, especially *Tatsuta*, do not fairly teach or suggest the claimed limitations that (i) said cavity is free of said adhesive layer (ii) which **directly** and hermetically bonds said chip and said substrate together. The first embodiment of *Tatsuta* illustrated in FIGs. 1-3 of the reference fails to teach or suggest the former limitation. *See* element 3 in FIGs. 1A-3B of *Tatsuta*. The second embodiment of *Tatsuta* illustrated in FIGs. 7-10 of the

reference fails to teach or suggest the latter limitation, because adhesive 43 (FIG. 7B) does not directly bond chip 2 to substrate 1. In the embodiment of FIGs. 7-10, adhesive 43 directly bonds substrate 1 to pressure holding member 4 which is not part of chip 1 as best seen in FIG. 7A.

As to claim 19, the applied references, especially *Tatsuta*, do not fairly teach or suggest the claimed limitations that (i) said cavity is free of said adhesive layer and (ii) said second bonding pads are spaced from a circumference of said cavity by said adhesive layer. *See* FIG. 3 of the instant application where it is disclosed that second bonding pads 60 are spaced from a circumference of cavity 58 by adhesive layer 62. The first embodiment of *Tatsuta* illustrated in FIGs. 1-3 of the reference fails to teach or suggest the former limitation. *See* element 3 in FIGs. 1A-3B of *Tatsuta*. The second embodiment of *Tatsuta* illustrated in FIGs. 7-10 of the reference fails to teach or suggest the latter limitation, because adhesive 43 (FIG. 7B) is not disposed between second bonding pads 22, 20 and the circumference of the cavity 17 as presently claimed.

As to claim 20, the applied references, especially *Tatsuta*, do not fairly teach or suggest the claimed limitations that (i) said cavity is free of said adhesive layer and (ii) said bonding pads are spaced from each other by said adhesive layer. *See* FIG. 4 of the instant application where it is disclosed that second bonding pads 60 are spaced from each other by adhesive layer 62. The first embodiment of *Tatsuta* illustrated in FIGs. 1-3 of the reference fails to teach or suggest the former limitation. *See* element 3 in FIGs. 1A-3B of *Tatsuta*. The second embodiment of *Tatsuta* illustrated in FIGs. 7-10 of the reference fails to teach or suggest the latter limitation, because second bonding pads 22, 20 of *Tatsuta* are spaced from each other by cavity 17, rather than adhesive layer 43 as presently claimed.

New Claim 12 is directed to a package structure with a cavity, which comprises a SAW chip having a first surface, a second surface opposite to the first surface, an interdigital transducer (IDT) disposed on the first surface, and a plurality of first bonding pads disposed around the interdigital transducer on the first surface; a multi-layer ceramic substrate having a hollow formed

therein and a plurality of second bonding pads disposed around the hollow and electrically connected to the first bonding pads, wherein the hollow and the plurality of second bonding pads correspond to the interdigital transducer and the plurality of first bonding pads, respectively; and **an adhesive layer formed around the hollow and between the first surface of the SAW chip and the multi-layer ceramic substrate for tightly bonding the SAW chip and the multi-layer ceramic substrate together, wherein the first surface of the SAW chip, the adhesive layer and the hollow of the multi-layer ceramic substrate together define a hermetic cavity such that the interdigital transducer of the SAW chip is disposed within the hermetic cavity.**

None of the cited references teach or suggest the highlighted limitation. The reference also fails to teach or suggest the claimed "multilayer ceramic substrate" as argued with respect to claim 1 and "SAW chip" as argued with respect to claim 2. Therefore, new Claim 12 is believed patentable over the cited references.

New Claims 13-17 are considered allowable for the reason advanced with respect to new Claim 12 from which they depend.

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

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To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

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